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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTORS: Stephan L. JOURDAN, et al.

SERIAL NO: 09/608,624

FILING DATE: June 30, 2000

TITLE: TRACE INDEXING VIA TRACE END ADDRESSES

ART UNIT: 2183

EXAMINER: Henry TSAI

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SUPPLEMENTAL APPEAL BRIEF

SIR:

This supplemental brief is in response to the Office Action mailed September 21, 2005, reopening prosecution in the above-identified application. The Appellant requests reinstatement of the appeal.

Response to new grounds of rejection

The above-identified Office Action (hereafter, "Office Action") raised new grounds of rejection under 35 USC § 101, 35 USC § 112, second paragraph, and 35 USC § 102. The Appellant's response follows.

Section 101

Claims 1-3, 20 and 22-27 were rejected under 35 USC § 101 as being directed to non-statutory subject matter. Specifically, the Examiner contends that the term "memory entry" used in the rejected claims may be reasonably interpreted as relating to "pages of a notebook" and that the term "trace" may be interpreted as a "line" or "path." Therefore, the Examiner argues, the claims do not relate to something tangibly embodied on a computer-readable medium and instead relate only to non-functional descriptive material. The claims are therefore non-statutory, according to the Examiner. See Office Action at page 3, item 3.

First, removing any possible ambiguity, "memory entry" is recited as a component of an apparatus in the rejected claims. Thus, even under the Examiner's severely strained interpretation, the claims recite at least an article of manufacture and are therefore statutory.

As to the Examiner's interpretation itself, the Appellant responds that while claims are to be given their broadest reasonable interpretation during examination, the interpretation must be consistent with the specification. See, e.g., MPEP § 2111: "During patent examination, the pending claims must be "given their broadest reasonable interpretation *consistent with the specification*" (citing In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000)) (emphasis added). Citing Ferguson Beauregard/Logic Controls v. Mega Systems, 350 F.3d 1327, 1338, 69 USPQ2d 1001, 1009 (Fed. Cir. 2003), the MPEP goes on to explain that "[i]t is the use of the words in the context of the written description and customarily by those skilled in the relevant art that accurately reflects the 'ordinary' and the 'customary' meaning of the terms in the claims" See MPEP § 2111.01(II).

Here, the Examiner has strayed markedly from the guidelines set forth by the above-cited authority. To interpret the claim term "memory entry" as a page from a notebook, and the term "trace" as a line or path is completely inconsistent with the specification, and is not what the person skilled in the art would understand to be meant. Instead, the person of ordinary skill in the computer-related arts understands a memory to be a component of a computer for electronically storing data. Many dictionaries recognize this meaning; one example is the popular online dictionary

www.dictionary.com, which defines a memory as "a unit of a computer that preserves data for retrieval."

Particularly when viewed in the context of the written description and the claims, the Examiner's interpretation of "memory entry" is painfully distorted and inaccurate. The claimed memory entry clearly is at least one of a machine or article of manufacture, or a component of a machine or article of manufacture, and is therefore statutory subject matter under § 101.

Section 112

Claims 1-3, 4-7, 9-19, 20 and 22-30 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

Concerning claim 1, the Examiner alleges that (1) "it is not clear how a trace can have a multi-entry and a single exit," that (2) "[t]he flow of a program can only have an [sic; it is assumed "one" is meant] entry in a trace," and that (3) "[s]ome more detailed descriptions are missing." See Office Action, page 5, item 6, par. 2. In response to points (1) and (3), it is observed that it is not the role of the claims to describe or explain the invention; that is the role of the written description. As to point (2), the Examiner's statement is palpably inaccurate. Program logic can be designed to have many entry points. A conditional branch is only example of how a program flow can be entered at multiple different points.

Concerning claim 3, the Examiner alleges that the term "'terminal instruction' was not well defined" (Office Action, page 5, item 6, par. 3). In response, it is again noted that the claims are not required to describe the invention, but to "particularly point out and distinctly claim" the invention. Claim 3 does so. A "terminal instruction" by its plain meaning is a last instruction; claim 3 says that the memory entry of claim 1 is indexed by an address of this last instruction. A reasonable interpretation of "indexed" in the context of the written description and claims is "indicated" or "pointed to." Claim 3 could not be more clear.

Concerning claim 4, the Examiner states, "it is not clear how to define 'complex blocks' and 'block prefixes' since the structural relationship between 'complex blocks',

'block prefixes', and the front-end system was not defined" (Office Action, page 5, par. 4). Here, again the Examiner seeks to force the role of the written description onto the claims, apparently taking the position that terms whose meanings are self-evident need to be bolstered with added description. As discussed previously, this is not required of the claims. Notwithstanding -- a "block prefix" is simply that – a prefix of a block. The prefixes are for blocks labeled "complex." The relationship between the complex blocks, their prefixes and the front-end system is that the complex blocks and block prefixes are elements of the front-end system, which is perfectly clearly from the fact that the language reciting the complex blocks and block prefixes follows "A front-end system for a processor, comprising:".

As to claim 6, the Examiner alleges that "it is not clear what is meant by 'blocks having a multiple-entry, single exit architecture' since the range of the blocks was not defined" (Office Action, page 5, par. 5). Here, the Examiner again seems to be relying on non-existent authority, or at least thoroughly misunderstanding the claims. No logical connection is apparent between "the range of the blocks" and the claimed multiple-entry, single exit architecture; certainly, no authority requires defining concepts ("the range of the blocks") seemingly invented by the Examiner and bearing no relationship to the claimed subject matter.

As to claim 20, the Examiner repeats the argument that the flow of a program "can only have an [sic; one?] entry." This is simply incorrect, as noted earlier.

Pursuant to 37 CFR § 1.116, cancellation of claim 22 without prejudice is requested.

As to claim 23, the Examiner alleges that the "last instruction" recited is unclear because "there exist many last instructions in the memory." Although it is not fully understood what is meant by the latter, in claim 23, "last instruction" refers to a last instruction in a trace, of which there is only one.

Section 102

Claims 1-3 and 38-40 were rejected under 35 USC § 102(b) as being anticipated by Kaylor (U.S. 5,492,276) ("Kaylor"). This rejection constitutes unmitigated error. Not only does the Kaylor reference not disclose the elements of the rejected claims as

required under § 102, it is not even remotely related to the same field as the present invention. The present invention, as disclosed and claimed, relates to computers, and in particular to processor front-ends and techniques for managing them. The Kaylor reference, by contrast, relates to plumbing. Not a single element in the Kaylor reference can fairly be found under any reasonable interpretation to correspond to any element of the rejected claims.

Claims 1, 2, 16, 20, 28, 29, 38 and 39 were rejected under 35 USC § 102(e) as being anticipated by Agarwal (US 5,966,541). Here, the Examiner repeats the arguments of the final rejection mailed January 4, 2005, which were addressed in the appeal brief filed June 28, 2005. Accordingly, the Appellant's arguments will not be repeated here.

Claim objections

Claims 4-7 were objected to for alleged informalities. The Appellant submits that claims 4-7 are easily understandable without the Examiner's proposed punctuation.

Conclusion

In view of the above, it is clear that the Examiner erred in the rejections and objections asserted in the Office Action. It is therefore respectfully requested that the Board reverse the Examiner, withdraw all rejections and objections, and allow claims 1-7, 9-20, 22-30 and 38-43.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

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